Please amend the claims as follows:

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1. (Previously Presented) An apparatus for collecting high-speed processor interconnect signals over a period of time sufficient for steady state effects to become manifest in as system under test, said apparatus comprising:

an input channel circuit for receiving all activity on a high speed processor interconnect in a system under test,

a preview pipeline circuit connected to monitor said input channel for capturing all occurrences of said high-speed processor interconnect signals at processor speed,

a trigger circuit maintaining a predetermined trigger value to compare against said all occurrences, and to trigger identification of all of said high-speed processor interconnect signals associated with each appearance of a trigger signal equivalent to said predetermined trigger value in said occurrences captured by said pipeline circuit and to pass each instance of said occurrences which are associated with a said appearance of a trigger signal as a word on to a compaction circuit, wherein said trigger may be set to at least one trigger value as desired by a user and wherein said trigger values correspond to processor ID values in said system under test,

a time stamp generating circuit for generating a time stamp value signal for each said occurrence and associating a one of said time stamp values associated with a one of said each occurrences,

said compaction circuit for eliminating any wasted space within said word and passing compacted sets of such words as an entry signal on to a high speed FIFO memory at said high speed processor interconnect speed, each of said words in said compacted set of words being passed with an associated time stamp value signal,

said high speed FIFO memory operating at said high-speed processor interconnect speed for receiving said entry signals at said high-speed processor

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interconnect speed and for providing that each of said entry signals is associated with a said associated one of said time stamp value signals, and for providing a said entry and its said associated time stamp value signals to an output channel.

2. (Previously Presented) The apparatus of claim 1, further comprising; a collector computer system having a channel connected to receive said entry signals from said output channel and to store them in a main memory for later flushing to a permanent memory system.

3. (Original) Apparatus as set forth in claim 2 wherein a console is associated with said collector computer system and wherein said console provides a user interface by which said trigger can be set to at least one trigger value as desired by a user at said console.

4. (Original) Apparatus as set forth in claim 3 wherein said trigger set to at least one trigger value as desired includes trigger values corresponding to address range values in said system under test.

5. (Original) Apparatus as set forth in claim 3 wherein said trigger set to at least one trigger value as desired includes trigger values corresponding to address/function values in said system under test.

6. (Canceled)

7. (Original) Apparatus as set forth in claim 3 wherein said trigger set to at least one trigger value as desired includes pulse occurrences on identified lines of said input channel.

8. (Previously Presented) Apparatus as set forth in claim 1 wherein said input channel comprises an interposer interposed between a processor on a

processor bus in a computer system under test and said preview pipeline circuit wherein said processor bus is said high-speed processor interconnect.

8. (Original) Apparatus as set forth in claim 1 wherein said FIFO memory has sufficient capacity for holding at least two kilo-entry signals.

9. (Original) Apparatus as set forth in claim 1 wherein said FIFO memory has sufficient capacity for holding between two kilo-entry and 16 kilo-entry signals.

10. (Original) Apparatus as set forth in claim 1 wherein said FIFO memory has sufficient capacity to handle anticipated burstiness of software in use on a system under test.

11. (Original) Apparatus as set forth in claim 1 wherein said compaction circuit comprises control logic settable to determine specific bytes of a word to be selected-down to.

12. (Original) Apparatus as set forth in claim 1 wherein said compaction circuit passing of an associated time stamp value signal with each word in an entry compacts said time stamp value signals such that for each entry signals associated with each word from said each entry only a predetermined one of said time stamp values is passed.

13. (Previously Presented) A method for collecting high speed processor signals over a period of time sufficient for steady state effects to be manifest in a tracing of such signals in a system under test, said method comprising:

a. connecting to a high speed interconnect from which to receive processor signals from one processor only in a multiprocessor system on an

input channel connected to said one processor's only connection to said input channel,

b. receiving signals from said high speed interconnect at a clock speed matching said high speed interconnect in a collector computer system,

c. setting up said collector computer system to receive said signals upon initiation of said collector computer system, whereupon said collector computer system monitors said input channel for said received signals and captures said received signals as input words,

d. generating a time stamp value for each input word, and associating each generated time stamp value with a said input word signal,

e. monitoring said input words for an appearance of a trigger signal said trigger signal identifying said one processor only, and

f. storing only entry word signals associated with each said appearance of a trigger signal during a tracing period into a high speed FIFO memory together with its associated time stamp value as entry signals.

~~15~~ 14. (Previously Presented) The method of claim ~~14~~ 13 further comprising an additional step:

g. passing entries from said FIFO to a collector system main memory for later flushing to permanent memory for study.

~~16~~ 15. (Original) The method of claim ~~14~~ 13 wherein in said connecting step (a) said connection to said high speed interconnect is made to a high speed processor bus and said processor signals are in a bus protocol format and wherein an additional step aligns each series of a bus protocol word series of signals into a single one of said entry words.

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17. (Original) The method of claim 14 wherein said entry word signals associated with each said trigger signal comprise a predetermined number of said entry word signals immediately preceding an occurrence of a trigger signal plus a predetermined number of said entry word signals immediately following said an occurrence of said a trigger signal.

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18. (Original) The method of claim 17 wherein at least one of said predetermined numbers of entry words is a zero.

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19. (Original) The method of claim 14 wherein said step (f) further comprises compacting said entry words associated with a said trigger signal prior to said storing.

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20. (Original) The method of claim 19 wherein said compacting comprises inputting said entry words associated with a said trigger signal into an array of select-down circuits, selecting only those bytes in a said entry word predetermined to contain data of interest, passing said selected down those bytes in an entry word predetermined to contain data of interest into a byte stuffer as an abbreviated entry word, and stuffing said abbreviated entry words into a stuffed entry word for transfer into a high speed FIFO memory.

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21. (Original) The method of claim 20 wherein said stuffing into a stuffed entry word comprises stuffing a plurality of abbreviated entry words into a stuffed entry word.

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